

VSC8228

VITESSE

Dual Channel Multirate Signal Conditioner and Retimer



FEATURES:

- ▶ Dual Clock and Data Recovery Architecture for Gigabit Ethernet and Fibre Channel Applications
- ▶ FibreTimer™ Configurable Clock Recovery Unit (CRU): Repeater, Retimer, or Bypassed
- ▶ Programmable Input Signal Equalization, Output De-emphasis, and Output Drive Levels
- ▶ Analog Signal Detect and Protocol Monitor Indicators
- ▶ Optional Half-rate SGMII Clock and Repeated Reference Clock Output
- ▶ Built In Self Test Which can Generate and Detect an Unframed 2⁷, 2²³, and 2³¹ Pseudorandom Bit Stream (PRBS), a User Defined Pattern, and the Fibre Channel CRPAT, CJTPAT, and CSPAT Patterns

APPLICATIONS:

- ▶ Fibre Channel Switches, Disk Arrays, RAID Subsystems, Host Bus Adapters
- ▶ Gigabit Ethernet Line Cards
- ▶ Blade Server Backplanes

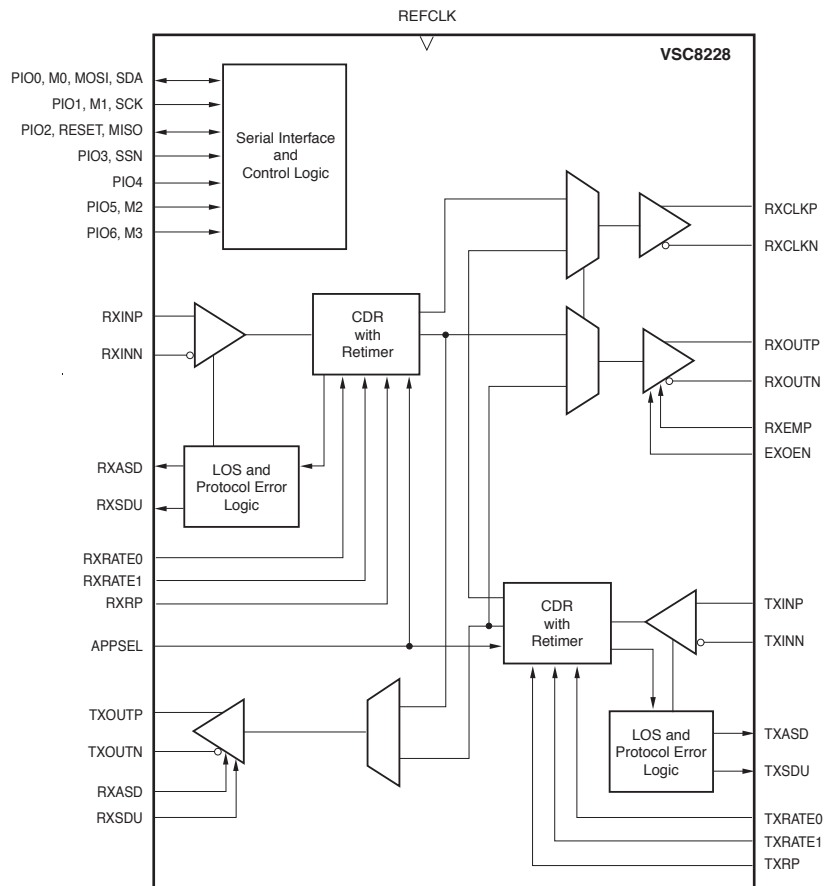
SPECIFICATIONS:

- ▶ Single 1.2 V and/or 1.8 V Supply
- ▶ 10mm x 10mm 64-pin TQFP Package
- ▶ SPI or Two-wire Serial Interface
- ▶ Typical Power: 360 mW

BENEFITS:

- ▶ Provides Fibre Channel and Gigabit Ethernet Signal Conditioning, Improving the Signal Integrity
- ▶ Offers flexible implementation. FibreTimer in Retimer Mode Minimizes the Jitter Generation, While Maintaining High Jitter Tolerance. In Repeater Mode Offers Low Latency Signal Cleanup. Bypass Mode Allows Support for Rates in not Directly by the CDR.
- ▶ Supports Extended Trace Lengths Over Copper Backplanes and Cables, Ideal for Backplane and Rack-to-rack Applications
- ▶ Supports enhanced receiver diagnostic capabilities.
- ▶ Provides SerDes to SGMII Gigabit Ethernet interface conversion.
- ▶ Enables Comprehensive System Diagnostic Capabilities. The Extended Pattern Support Reduces the Need for External test Equipment

BLOCK DIAGRAM:



Dual Channel Multirate Signal Conditioner and Retimer

GENERAL DESCRIPTION:



The VSC8228 is a dual repeater/retimer for Fibre Channel, Gigabit Ethernet, SONET/SDH, and Infiniband applications. The VSC8228 contains dual FibreTimer™ clock recovery units (CRU) for bidirectional signal conditioning in system interconnect and serial backplane applications. The device supports rates from 125 Mbps up to 4.25 Gbps. Using a single reference clock for acquisition, the VSC8228 retransmits the incoming serial data synchronously to the reference clock in retimer mode or to the incoming data in repeater mode. In the retimer mode, add/drop elasticity buffers insert/delete Fibre Channel fill words to account for timing differences in the incoming data and local reference clock.

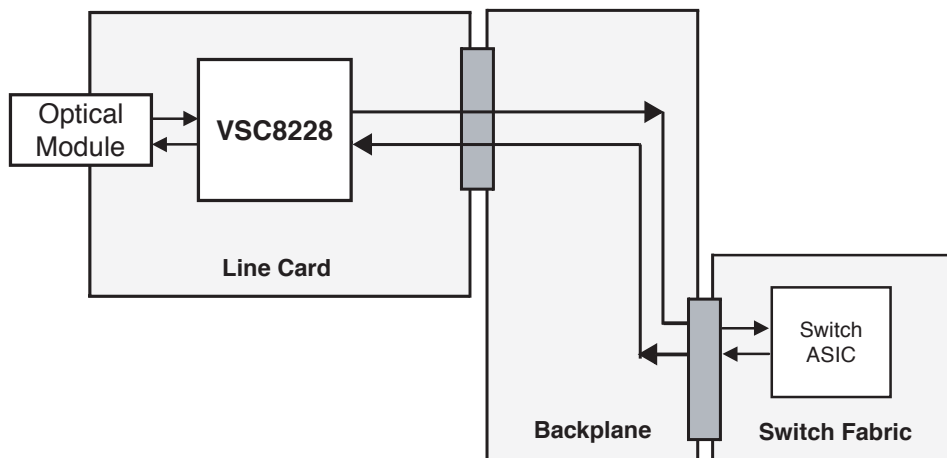
An analog signal detect function is integrated into both channels. In the retimer mode, the device monitors the incoming data for run-length violations and K28.5- symbols. The inputs on both the transmit and receive channels can be looped back to the outputs of the opposite channels for diagnostic purposes. The device provides a built-in pattern

generator and checker. An optional half-rate clock for SGMII applications is provided on the receive channel output.

A high degree of signal integrity is maintained via differential I/O, on-chip input and output terminations, input equalization, and output de-emphasis. The programmable input equalization circuit compensates for the frequency limitations of long printed circuit board (PCB) traces, backplanes, connectors, and cables. Equalization, de-emphasis, output drive levels, data rate, and other features are configured through industry standard serial interfaces (Two-wire or SPI).

The device may be powered from a single 1.2 V supply, single 1.8 V supply, or both a 1.2 V and 1.8 V supply. The 1.8 V supply is required to meet the LVPECL output swing levels. The device has current-mode logic (CML) inputs and outputs that can be AC-coupled for LVPECL and LVDS compatibility. The IC is packaged in a compact 10mm x 10mm, 64-pin TQFP package. Typical power dissipation for a 1.2 V supply is 360 mW.

APPLICATION DIAGRAM:



For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com or contact Vitesse Sales at (800) VITESSE or sales@vitesse.com

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